REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 21 through 28 remain in this case. Claims 1 through 20 were previously canceled. Claims 21, 24, and 25 are amended. Claims 27 and 28 are added.

In the Office Action of December 3, 2007, the Examiner objected to claim 24 as depending on a rejected claim, but indicated that claim 24 was otherwise directed to allowable subject matter.[1] Claim 24 is amended in this Submission to be placed in independent form, incorporating all of the limitations of previous claim 21. Applicants submit that amended claim 24 is therefore in condition for allowance.

Claim 25 is amended to now depend on amended claim 24; claim 26 previously depended on claim 25, and still does. Accordingly, Applicants submit that, upon entry of this amendment, claims 25 and 26 will also be in condition for allowance.

In the Office Action of December 3, 2007, the Examiner finally rejected claims 21 through 23, 25, and 26 as unpatentable over the admitted prior art in view of the Fujioka reference[2]. The Examiner asserted that it would have been obvious to have combined the bias voltage generator of elements 61 through 66, as taught by Fujioka, into the multistage differential amplifier shown as the admitted prior art of Figure 2, so that the Fujioka bias voltage generator produced the voltage V_{BIAS} used in each of the stages of the Figure 2 circuit, in order to provide a stable constant bias voltage.[3]

Claim 21 is amended in this Submission to clarify its patentability. Amended claim 21 now recites that the diode-connected transistor of the temperature responsive unit in the claimed voltage regulator has a voltage-temperature response similar to that of the emitter-follower

---

[1] Office Action of December 3, 2007, page 4.
[2] U.S. Patent No. 6,020,781, issued February 1, 2000 to Fujioka.
[3] Office Action, *supra,* page 2.

output transistors in the first amplifier stage. Applicants submit that the specification clearly supports this amendment to claim 21.[4] No new matter is presented.

Applicants submit that amended claim 21 and its dependent claims are patentably distinct over the admitted prior art in proper combination with the Fujioka reference.

First, Applicants submit that the combined teachings of the applied prior art fall short of the requirements of amended claim 21. As noted above, amended claim 21 now requires that the diode-connected transistor in the temperature responsive unit of the voltage regulator have a voltage-temperature response similar to that of the emitter follower output transistors in the first amplifier stage. Even if one were to combine the Fujioka teachings with the admitted prior art in the manner asserted by the Examiner,[5] that combination of teachings would not reach all of the limitations of amended claim 21, as will now be explained.

As noted above, the Examiner asserted that the bias voltage generator circuit consisting of elements 61 through 65 of Figure 1 of the Fujioka reference corresponds to the voltage regulator of claim 21, with the temperature responsive unit of the claim being met by transistor 64 and resistors 65, 66.[6] As evident from the reference itself,[7] its transistor 64 is an n-channel MOS transistor that has its drain connected to its gate. On the other hand, the emitter follower transistors in the differential amplifiers in the admitted prior art circuit of Figure 2 are bipolar transistors.[8] Not only does the Fujioka reference nowhere mention the matching of the voltage-temperature characteristic of its transistor 64 to any other transistor in *its* circuit, it is a virtual certainty that the voltage-temperature characteristic of nMOS transistor 64 of the Fujioka reference would not match the voltage-temperature characteristic of the bipolar emitter follower transistors 152, 182 of the Figure 2 circuit, if the Examiner's combination were made. Accordingly, the combination of the Fujioka teachings with the admitted prior art in the manner

---

[4] Specification of S.N. 10/695,604, page 10, lines 1 through 21; page 11, line 16 through page 12, line 6; page 12, line 22 through page 13, line 12; page 13, line 27 through page 14, line 17; page 15, line 26 through page 16, line 8.
[5] Applicants do not, by this argument, admit that such a combination is suggested by the prior art or within the ordinary creativity of the skilled artisan.
[6] Office Action, *supra,* pages 2 and 3.
[7] Fujioka, *supra,* column 6, lines 21 through 40; Figure 1.
[8] Specification, *supra,* page 5, line 19 through page 6, line 2; Figure 2.

alleged by the Examiner will fall short of the requirements of amended claim 21 and its dependent claims.

Secondly, Applicants submit that there is no motivation or suggestion from the prior art, or from within the ordinary creativity of the skilled artisan, to modify the teachings of this combined prior art in order to reach the requirements of amended claim 21.

The Examiner asserted that the motivation to combine the Fujioka reference with the admitted prior art is to "provid[e] a stable constant bias voltage".[9] However, a stable bias voltage from the temperature-responsive unit is *undesirable* according to the invention of claim 21. As discussed in the specification of this application,[10] conventional multistage LVDS output stages, such as that shown in the admitted prior art of Figure 2, used common-mode feedback from the output of each stage to regulate the common mode of that stage, thus compensating for base-emitter voltage variations with temperature and ensuring proper bias in succeeding stages. However, the alleged combination of the Fujioka circuit into this admitted prior art will not accomplish this result. As disclosed by the Fujioka reference itself:

> The drain and gate electrodes of the nMOS transistor 64 are short-circuited in order *to prevent the internal power-supply potential Vii from changing according to ambient temperature.*[11]

Assuming that the Fujioka circuit accomplishes this goal, the temperature-stable output voltage produced by the Fujioka circuit would therefore be useless as a feedback signal to regulate the common-mode of a differential amplifier stage. In contrast, the temperature-responsive unit of claim 21 produces a feedback level that varies with temperature in the same way as the base-emitter voltage of the emitter follower transistors in the differential amplifier stages.[12] This function is reflected in the claim term "temperature-responsive unit", and is also reflected in the claim limitation that the diode-connected transistor in this temperature-responsive unit has a voltage-temperature response similar to that of the emitter-follower output transistors in the first amplifier stage.

---

[9] Office Action, *supra,* page 2.
[10] Specification, *supra,* page 8, lines 3 through 16.
[11] Fujioka, *supra,* column 6, lines 35 through 40 (emphasis added).
[12] *See* specification, *supra,* page 10, lines 1 through 21; page 11, line 16 through page 12, line 6; page 12, line 22 through page 13, line 12; page 13, line 27 through page 14, line 17; page 15, line 26 through page 16, line 8.

Therefore, given that the stated goal of the Fujioka circuit is to produce a voltage that does not vary at all with temperature, there can be no suggestion from the prior art, or within the ordinary creativity of the person of ordinary skill in the art, to modify the combined teachings of the Fujioka reference and the admitted prior art so that the diode-connected transistor has a voltage-temperature response similar to that of an emitter follower in an amplifier stage. Accordingly, Applicants submit that it would not have been obvious to a person of ordinary skill in the art to modify those combined teachings in such a manner as to arrive at the invention of amended claim 21 and its dependent claims.

Furthermore, Applicants submit that the substantial advantages provided by the differential amplifier of amended claim 21 and its dependent claims indicate the patentability of those claims. As described in the specification, conventional multistage differential amplifiers required common-mode voltage sensing and feedback control circuits for each stage, in order to control common-mode voltage variations.[13] According to the invention of amended claim 21, the temperature responsive unit in the voltage regulator is based on a diode-connected transistor that has a similar voltage-temperature response to the emitter follower output transistors in the amplifier stage, according to which the common-mode transistor in the amplifier stage is controlled. Sensing of the output common-mode voltage at each stage is therefore not necessary according to the claimed circuit. Not only does the recited voltage regulator circuit therefore avoid resistors and the like for sensing the common-mode output of the amplifier stage, but this voltage regulator circuit is also capable of regulating the common-mode voltage of multiple amplifier stages.[14] This savings in circuit complexity and chip area directly results from the ability of the claimed voltage regulator to mimic, in voltage-temperature response, the emitter follower transistors in the amplifier stage. Because these substantial advantages stem directly from the differences between the amplifier of amended claim 21 and its dependent claims, Applicants submit that these advantages support the patentability of those claims.

Claims 27 and 28 are added to more completely cover all aspects of Applicants' invention. Claim 27 further requires, relative to amended claim 21 upon which it depends, that

[13] Specification, *supra,* page 2, lines 1 through 6.
[14] *See* specification, *supra,* page 15, line 26 through page 16, line 8; *see also* new claim 27.

the voltage regulator is also coupled to control the second common-mode transistor in the second amplifier stage, and that the diode-connected transistor in the voltage regulator has a has a voltage-temperature response similar to that of each of the second pair of emitter-follower output transistors in that second amplifier stage.[15] Claim 28 further requires, relative to claim 27, the presence of a third amplifier stage in similar manner as recited in previously presented claim 26. No new matter is presented by these new claims, given the clear support noted above.

For the same reasons as discussed above relative to amended claim 21, Applicants submit that claims 27 and 28 are patentably distinct over the applied prior art. In addition, Applicants submit that claims 27 and 28 are further patentably distinct over this prior art because there is especially no suggestion from the cited teachings, or within the ordinary creativity of the person of ordinary skill in the art, to use the Fujioka teachings as a voltage regulator to control the common-mode transistors in each of multiple stages, given that the output of the Fujioka reference bias circuit does not produce a common-mode compensating voltage in the first place. Applicants therefore submit that new claims 27 and 28 are in condition for allowance.

For these reasons, Applicants respectfully submit that all claims in this case will be in condition for allowance, upon entry of this amendment. Favorable reconsideration of this application in its continued examination is therefore respectfully requested.

Respectfully submitted,
/Rodney M. Anderson/
Rodney M. Anderson
Registry No. 31,939
Attorney for Applicants

Anderson, Levine & Lintel, L.L.P.
14785 Preston Road, Suite 650
Dallas, Texas 75254
(972) 664-9554

[15] *See* specification, *supra,* page 15, line 26 through page 16, line 8; Figure 7.